Center of Excellence in Nanotechnology (CoEN)

Special Lecture on

"Beyond CMOS Technology and Evolutionary Architectures"
on

Tuesday, 12th October 2010 at 2:00 PM

by
Prof. Pinaki Mazumder, University of Michigan, USA

Venue: Room 102, Outreach Building, Asian Institute of Technology

Abstract

Conventional shrinking methods to improve Very Large Scale Integration (VLSI) chip performance by continual scaling of device and interconnect geometries may allow Complementary Metal Oxide Semiconductor (CMOS) juggernaut to reach about 22 nm nodes. During the post-shrinking era, a horde of mesoscopic and nanoscale technologies such as resonant quantum tunneling diodes, spoof plasmon-based transistors, ionic transport based crossbar structures, nanomagnetic logic, grapheme transistors, self-assembled array of quantum dots, and molecular devices are likely to emerge as commercially viable technologies in order to sustain the demands for exponential economic growth throughout the first quarter of
the twenty first Century.

Quantum tunneling in nanometric devices augurs a revolutionary shift of paradigm for circuit and Computer Aided Design (CAD) tools design that must account for quantum effects as well as local interactions between self-assembled circuit elements. These circuit elements may consist of a 2- dimensional array of self-organized quantum dots that can be instrumented to perform cellular automata class of algorithms or a 3-dimensional array of self-organized nanowires to perform a random Boolean network (RBN) class of algorithms. The talk will also briefly introduce neuromorphic nanoarchitectures consisting of 2-D array of amorphous-Silicon based memristor devices and also THz digital systems deploying spoof surface plasmon polariton (SSPP).

Biography

Prof. Pinaki Mazumder (http://www.eecs.umich.edu/~mazum) received his Ph.D. from the University of Illinois at Urbana-Champaign in 1988. He is a Professor of Electrical Engineering and Computer Science at the University of Michigan. Currently, he is on leave for two years from the UM to serve as the lead Program Director of the Emerging Models and Technologies Program at the US National Science Foundation. He had worked for six years in various industrial R&D centers including AT&T Bell Laboratories, where in 1985 he began the CONES project - the first C modeling based VLSI synthesis tool. He has also worked at Bharat Electronics Limited, India's premiere electronics company, where he developed several high-speed and high-voltage analog integrated circuits intended for consumer electronics products. He has published over 230 technical papers and 4 books on various aspects of VLSI research works. His research interest includes current problems in Nanoscale CMOS VLSI design, CAD tools and circuit designs for emerging technologies including Quantum MOS and resonant tunneling devices, semiconductor memory systems, and physical synthesis of VLSI chips. Dr. Mazumder is a recipient of Digital's Incentives for Excellence Award, BF Goodrich National Collegiate Invention Award, and DARPA Research Excellence Award. Dr. Mazumder is an AAAS Fellow (2007) and an IEEE Fellow (1999) for his contributions to the field of VLSI.